(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 583 841 A2**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **93202413.6**

(51) Int. Cl.5: **H02M 3/337**

(22) Date of filing: **17.08.93**

(30) Priority: **20.08.92 US 932839**

(43) Date of publication of application:
23.02.94 Bulletin 94/08

(84) Designated Contracting States:
BE DE ES FR GB IT NL

(71) Applicant: **PHILIPS ELECTRONICS N.V.**
Groenewoudseweg 1
NL-5621 BA Eindhoven(NL)

(72) Inventor: **Bandel, Michael**
c/o Int. Octrooibureau B.V.,
Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

(74) Representative: **Evers, Johannes Hubertus Maria et al**
INTERNATIONAAL OCTROOIBUREAU B.V
Prof. Holstlaan 6
NL-5656 AA Eindhoven (NL)

(54) **Switch mode power supply.**

(57) A switch mode power supply for a ballast having a power factor controller and providing a regulated D.C. output voltage. The controller is responsive to a control input signal which includes a sensed signal added to a varying offset. The sensed signal is representative of the current flow through a switching device of the power supply. The offset is varied based on the regulated D.C. voltage output.

EP 0 583 841 A2

This invention relates to a switch mode power supply incorporating power factor control circuitry. The invention also relates to a ballast for operating a discharge lamp.

Conventional power factor controllers such as model MC34261 and MC33261 available from Motorola Inc. of Phoenix, Arizona are particularly designed for use in a switch mode power supply of an electronic ballast. The power supply serves to provide a regulated D.C. voltage to power the inverter (commutator) of the ballast.

Generally, the regulated D.C. voltage appears across one or more electrolytic capacitors of the power supply or inverter of the ballast. During no-load or light load conditions of the ballast, that is, when there is substantially no lamp load to draw an appreciable amount of current from the one or more electrolytic capacitors, overcharging of the one or more electrolytic capacitors can occur. Such overcharging makes it more difficult to regulate the D.C. voltage and can damage the capacitor(s) as well as other components (e.g. transistors) of the inverter.

Overcharging of the one or more electrolytic capacitors during no-load conditions (which typically occur during pre-ignition of the ballast or when the load becomes disconnected from the ballast) can be minimized by turning a switch of the switch mode power supply OFF more quickly to minimize the amount of energy transferred to the electrolytic capacitor(s). In other words, the excessive build up of charge across the one or more capacitors during no-load and light load conditions can be substantially eliminated by turning the switch OFF more quickly.

The power factor controller determines when to turn the switch OFF based, in part, on a current sensed signal representative of the current flow through the switch. This signal is fed into a current sensed input of the controller. In order to increase the speed at which the switch turns OFF thereby minimizing potential overcharge of the electrolytic capacitor(s), a passive (i.e. constant) offset is added to the current sensed signal.

The enhanced sensitivity of the power factor controller to no-load and lightly loaded conditions through provision of a constant offset results in a higher switching frequency of the switch-mode power supply. The amount of energy transferred to the electrolytic capacitor(s) is reduced thereby avoiding an excessive build up of charge across the latter. The constant offset, however, can also reduce the power factor of the ballast and, in particular, leads to a higher than desired total harmonic distortion (THD) level in current drawn by the ballast.

Accordingly, it is desirable to provide a power factor controller which is sensitive to no-load and light load conditions of the lamp ballast to prevent overcharging of the electrolytic capacitor(s) while minimizing the THD level in current drawn by the ballast.

Generally speaking, in accordance with a first aspect of the invention, a switch mode power supply includes a current source for supplying current to at least one capacitor for providing an output voltage, a switching device for conditioning current supplied to the output, a controller responsive to a control signal for controlling conditioning by the switching device of current supplied to the at least one capacitor and sensing circuitry for producing the control signal. The control signal includes a sensed signal representing current flow through the switching device and a varying (active) offset based on the output voltage. In accordance with this aspect of the invention, the current source includes a choke responsive to the switching device for supplying current to the output.

By providing an active rather than a passive offset as part of the control signal, the switching device is turned OFF much more quickly. The offset is only of a sufficient magnitude to significantly effect the speed at which the switching device turns OFF during no load conditions resulting in a lower THD while preventing overcharging of the one or more capacitors at the output of the switch mode power supply. Through enhanced sensitivity to no-load conditions, the switch mode power supply is able to maintain a relatively high constant power factor.

For a fuller understanding of the invention, reference is had to the following description taken in connection with the accompanying drawings, in which:

FIG. 1 is a schematic diagram of a ballast circuit in accordance with the invention;

FIG. 2 is a more detailed schematic diagram of FIG. 1;

FIG. 3 is a block diagram of a conventional power factor controller; and

FIG. 4 is a block diagram of a conventional integrated circuit serving as a zener diode.

As shown in FIG. 1, a ballast circuit 20 includes an electromagnetic interference (EMI) suppression filter 23. Filter 23 has a pair of input terminals 10 to which a voltage such as, but not limited to, 277 volts, 60 hertz is applied. Filter 23 filters high frequency components inputted thereto lowering conducted and radiated EMI. The output of filter 23 provided at a pair of terminals 24 and 25 is supplied to a full wave rectifier 30 which includes diodes D_1, D_2, D_3 and D_4. The anode of diode D_1 and cathode of diode D_2 are connected to terminal 24. The anode of diode D_3 and cathode of diode D_4 are connected to terminal 25. The output of rectifier 30 (i.e. rectified A.C. signal) at a pair of

output terminals 31 and 32 is supplied to a boost converter 40. The cathodes of diodes D_1 and D_3 are connected to terminal 31. The anodes of diodes D2 and D4 are connected to terminal 32.

Converter 40 boosts the magnitude of the rectified A.C. signal supplied by rectifier 30 and produces at a pair of output terminals 41 and 42 a regulated D.C. voltage supply. Boost converter 40 includes a choke L3, a diode D_5 the anode of which is connected to one end of choke L3. The other end of choke L3 is connected to output terminal 31 of rectifier 30. The output of boost converter 40 at output terminals 41, 42 is applied across an electrolytic (boosting) capacitor CE, one end of which is connected to the cathode of diode D_5. A transistor (switch) Q1 is connected to the junction between choke L3 and the anode of diode D_5. The other end of transistor Q1 is connected to the junction between the other end of capacitor CE, output terminal 32 of rectifier 30 and output terminal 42.

A preconditioner control 50, which is powered by a D.C. supply voltage V, controls the switching duration and frequency of transistor Q1. Preconditioner control 50 is preferably, but not limited to, a Motorola MC33261 Power Factor Controller Integrated Circuit from Motorola Inc. of Phoenix, Arizona. Transistor Q1 is preferably a MOSFET, the gate of which is connected to preconditioner control 50. Rectifier 30 and boost converter 40, including preconditioner control 50, form a preconditioner 80 (switch mode power supply) for ballast circuit 20. Output terminals 41 and 42 of boost converter 40 also serve as the output for preconditioner 80 across which a regulated D.C. voltage is produced.

A lamp drive 90, which is supplied with the regulated D.C. voltage outputted by preconditioner 80, includes a half bridge inverter controlled by a level shifter 60 and a half-bridge drive 70. The half bridge inverter includes a pair of transistors Q6 and Q7, which serve as switches, a pair of capacitors C5 and C6 and a transformer T1. Preferably, but not necessarily, half-bridge drive 70 produces a square wave driving signal to drive transistor Q7 and has a 50-50 duty cycle. Level shifter 60 inverts the driving signal supplied to transistor Q7 for driving transistor Q6. The driving signals produced by level shifter 60 and half-bridge drive 70 are approximately 180° out of phase with each other so as to prevent conduction of transistors Q6 and Q7 at the same time, respectively.

A source S of transistor Q6 and one end of level shifter 60 are connected to output terminal 41 of boost converter 40. A drain D of transistor Q6 is connected to a terminal A. The other end of level shifter 60, one end of half-bridge drive 70 and a source S of transistor Q7 are also are connected to terminal A. The other end of half-bridge drive 70 and a drain D of transistor Q7 are connected to output terminal 42 of boost converter 40. Capacitor C5 is connected at one end to output terminal 41. The other end of capacitor C5 and one end of capacitor C6 are connected to a terminal B. The other end of capacitor C6 is connected to output terminal 42.

A primary winding Tp of transformer T1 is connected to terminals A and B. A secondary winding TS of transformer T1 is connected at one end to an inductor L7, the latter of which generally represents either the leakage inductance of transformer T1 or a discrete choke. Connected to the other end of inductor L7 is one end of a capacitor C10 and one end of a lamp load LL. Lamp load LL can include any combination of lamps and is shown, but not limited to, the series combination of two fluorescent lamps LL1 and LL2. The other ends of capacitor C10 and lamp load LL are connected to the other end of secondary winding Ts.

During no-load conditions electrolytic capacitor CE can overcharge resulting in damage to electrolytic capacitor CE as well as other components in lamp drive 90 such as, but not limited to, transistors Q6 and Q7. The overcharged state of electrolytic capacitor CE arises from choke L3 pumping (supplying) too much current (energy) to electrolytic capacitor CE. The amount of current supplied to electrolytic capacitor CE by choke L3 is determined by the switching duration and frequency of transistor Q1 which in turn is controlled by preconditioner control 50. It is therefore essential, as provided by the present invention and further discussed below, that preconditioner control 50 be extremely sensitive to no-load conditions in order to prevent the voltage across electrolytic capacitor CE from reaching unsafe levels without drawing a ballast current having an undesirable THD level (i.e. maintaining an acceptably high power factor).

A more detailed schematic diagram of ballast circuit 20 including the construction of EMI suppression filter 23 preconditioner control 50, level shifter 60 and half-bridge drive 70 is shown in FIG. 2.

Referring once again to FIG. 1, the rectified A.C. (i.e. pulsating D.C.) signal supplied to preconditioner 80 from diode bridge rectifier 30 is boosted in magnitude by choke L3 and diode D5 to charge capacitors CE, C5 and C6. In FIG. 1, capacitor CE is separate from capacitors C5 and C6, capacitor CE being a large electrolytic capacitor in the range of 5 to 100 microfarads. Capacitors C5 and C6 are high frequency bridge capacitors. Since capacitor CE is in parallel with the series combination of capacitors C5 and C6, these three capacitors can be reconfigured as capacitors C5' and C6'as shown in FIG. 2. The potential overvoltage condition of capacitor CE of FIG. 1 should therefore

be viewed as the potential overvoltage condition of capacitors C5' and C6' of FIG. 2 which is addressed by the present invention as discussed below.

Rectifier 30 is constructed similar to and with the same elements as shown in FIG. 1. Preconditioner control 50 includes a preconditioner integrated circuit (IC) chip IC1 operating in an asynchronous mode (i.e. not in synchronism with the A.C. voltage (V_{LN}) inputted to ballast circuit 20). Chip IC1 has four control input signals.

The first control input signal flows into pin 3 of chip IC1 from the rectified A.C. line through a resistor divider network including three resistors R1, R21, and R2 and a capacitor 13. This first control input signal represents the rectified A.C. voltage signal as an input to chip IC1.

The second control input signal flows into pin 5 of chip IC1, and represents the current flow of choke L3. This second control input signal is used to turn ON transistor Q1 when the current flow through choke L3 is about zero. Chip IC1, responsive to the second control input signal, produces a driving signal through a resistor R4 to turn ON transistor Q1.

The third control input signal is based on a resistor divider formed from resistors R6, R24 and R9, enters chip IC1 at pin 1 and is filtered by a capacitor C16. The third control input signal is a D.C. feedback signal to chip IC1 and represents the D.C. level across the output of preconditioner 80.

The fourth control input signal represents current passing through transistor Q1 and is determined based on resistor R5 which monitors all currents to Q1. At the junction between a resistor R23 and a capacitor C15, which serves as a lowpass filter, the fourth control input signal is fed into pin 4 of chip IC1. Responsive to a combination of the first, third and fourth control input signals, chip IC1 turns OFF transistor Q1 through the signal produced at pin 7 of chip IC1.

Preconditioner control 50 also includes an active offset circuit having an integrated circuit chip IC3, three resistors R30, R31 and R35 and a pair of diodes D13 and D14 which together limit the peak amplitude of the D.C. voltage across capacitors C5' and C6' at the time ballast 20 is turned ON, during operation of ballast 20 before lamp ignition and whenever ballast 20 is otherwise under a no-load (including light load) condition. This portion of preconditioner control 50 functions as a comparator which injects an active D.C. offset current (further discussed below) into pin 4 of chip IC1 when the voltage at pin 2 of chip IC1 drops below a threshold level.

Preconditioner 80 is an up-converter and boosts the rectified A.C. input voltage as follows. When transistor Q6 (which serves as a switch) is closed, choke L3 is short circuited to ground. Current flows through choke L3. Transistor Q1 is then opened (turned OFF). Choke L3 with transistor Q1 open transfers (pumps) stored energy (current) through diode D5 into capacitor CE of FIG. 1 or capacitors Q5' and Q6' of FIG. 2. The amount of energy transferred to capacitor CE of FIG. 1 or capacitor C5' and C6' of FIG. 2 is based on the time during which transistor Q1 is turned ON, that is, based on the frequency and duration of the driving signal supplied to the gate of transistor Q1 through resistor R4 by chip IC1. Asynchronous operation of transistor Q_1 with respect to voltage V_{LN} results.

Choke L3 operates in a discontinuous mode, that is, the current through choke L3 during each cycle is reduced to substantially zero before a new cycle is initiated. The frequency at which transistor Q1 is turned ON and OFF is varied by preconditioner control 50 so that the peak current through choke L3 is kept constant as set by resistor R5 (in FIG. 2). The D.C. voltage across capacitors C5', C6' (in FIG. 2) is kept constant so as to prevent these capacitors from overcharging and is set by the feedback network of resistors R6, R24 and R9 and capacitor C16. Resistors R26 and R10 are connected to the input of choke L3 and provide a D.C. bias as the initial power supply for half bridge drive 70 and an integrated circuit chip IC2 and as the bias for chip IC3 through resistor R31. Chip IC2 of half bridge drive 70 is a CMOS 555 timer which can be turned ON with a very low D.C. current in the order of 1 milliamp supplied via resistors R26 and R10.

Once, the half-bridge inverter is operating, the low voltage (snubber) power supply for chip IC2 is provided to chip IC2 through a pair of capacitors C21 and C23, a pair of diodes D16 and D15 and a zener diode D11. Chip IC2 has a limited output drive capacity. To increase this capacity, a pair of transistors Q4 and Q5 are used to help drive both half-bridge drive 70 and level shifter 60. A square wave signal from chip IC2 via transistors Q4, Q5 is supplied through resistor R17 and diode D17 to the gate of transistor Q7. Diode D17 in parallel with resistor R17 operates as a fast turnoff diode for quick discharge at the gate of transistor Q7. Resistor R17 and the internal gate capacitance of transistor Q7 provide a delay for turning ON transistor Q7. A controlled turn ON and a quick turn OFF of transistor Q7 is therefore provided. The signal present at the emitters of transistors Q4 and Q5 is also used to drive transistor Q2 of level shifter 60.

Level shifter 60 operates as follows: When transistor Q7 is turned ON, capacitor C7 is connected to ground through transistor Q7. Capacitor C7 is charged through resistor R11 and diode D6 from

the low voltage power supply of chip IC2 (i.e. junction of zener diode D11 and capacitor C21). During the period of time that transistor Q7 is turned ON, capacitor C7 becomes fully charged to the low voltage power supply voltage. Concurrently, the gate of transistor Q6 has been pulled to ground potential by diode D7, resistors R14 and R15 and transistor Q2.

Transistor Q2 can be viewed as being in parallel with transistor Q7 so that transistors Q2 and Q7 are turned ON and turned OFF at the same time. When transistors Q2 and Q7 are turned OFF, the stored charge of transistor Q7 is applied at the junction of the source of transistor Q6 and the drain of transistor Q7. This junction is now charged to the low voltage power supply. Resistor R12 quickly turns on the base of transistor Q3 so that charge can be transferred from capacitor C7 into the gate capacitance of transistor Q6 through transistor Q3 and resistor R13. Transistor Q6 is turned ON permitting current to flow therethrough.

Transistors Q6 and Q7 have internal diodes (not shown). These diodes, which can either be internal or external to the transistors, permit inductive currents to flow through transistors Q6 and Q7 at the initial turn ON and turn OFF of transistors Q6 and Q7.

Preferably, capacitors C5' and C6' are electrolytic capacitors having a pair of discharge resistors R5' and R6' in parallel, respectively. Transformer T1 is a leakage transformer, that is, having a leakage inductor of inductance L_M which serves as the ballast for lamp load LL (i.e. to limit steady state current flow through the lamp load). Alternatively, when transformer T1 has little or no leakage inductance an external inductor of inductance L_M is required for ballast purposes. Three windings T_{H1}, T_{H2} and T_{H3} provide the necessary current for heating the filaments of lamps LL1 and LL2 during ignition and steady state operation. In series with windings T_{H1}, T_{H2} and T_{H3} are inductors L4, L5 and L6, respectively, for limiting the current in the lamp filaments.

Transformer T1 has a main secondary winding T_M. A resonant capacitor C10 is in series with inductor L7 and reflects back to the primary winding of transformer T1 as a series LC combination across the half-bridge inverter. A capacitor C11 serves as a D.C. blocking capacitor to prevent rectification if this should occur within the lamp load. In parallel with capacitor C11 is a resistor R34 for discharge of capacitor C11 should rectification occur. Blocking capacitor C11 has substantially no ballast function (i.e. to limit steady state current flow through the lamp load) and typically has a minimal voltage drop in the order of several volts. A capacitor C12 serves as a bypass capacitor for lamp LL2 and is used during lamp starting as part of a normal lamp sequence starting scheme.

In accordance with the invention, an active offset is supplied to the current sense input (pin 4) of chip IC1. Referring once again to FIG. 2, by providing the active offset, chip IC1 is more responsive to no-load conditions by more quickly turning transistor Q1 OFF and thereby increasing the switching frequency of transistor Q1. The increased frequency limits the amount of energy which can be stored by choke L3 and transferred by choke L3 to electrolytic capacitor CE of FIG. 1 and capacitors C5' and C6' of FIG. 2.

FIG. 3 is a block diagram of chip IC1 which is well known in the art and readily available from Motorola, Inc. of Phoenix, Arizona under part numbers MC34261 and MC33261 Power Factor Controller. Chip IC1 determines when to turn transistor Q1 OFF based on control inputs to pins 1, 3 and 4. Pin 3 receives a signal representing the rectified A.C. voltage which is supplied to a multiplier 100 of chip IC1.

The D.C. voltage signal supplied to the voltage feedback input (pin 1) of chip IC1 is fed into an inverting input of an error amplifier 110 of chip IC1. The non-inverting input of error amplifier 110 is connected to a 2.5 volt reference. Consequently, whenever the voltage across capacitors C5' and C6' is too high, (i.e. overcharged), the output of error amplifier 110 will decrease. This output is supplied to both multiplier 100 and outputted at pin 2 of chip IC1 as a compensating signal. As particularly shown in FIG. 2, capacitor C16 is connected between pins 1 and 2 of chip IC1. Consequently, when the output voltage of error amplifier 110 decreases, the compensating signal outputted at pin 2 is fed back through capacitor C16 to the inverting input of error amplifier 110 in order to maintain the voltage at pin 1 of error amplifier 110 at approximately 2.5 volts. Similarly, when the voltage across capacitors C5' and C6' are lower than desired, the compensating signal into pin 1 will raise the inverting input (pin 1 voltage) of error amplifier 110 to approximately 2.5 volts.

The output of multiplier 100 represents a combination of the rectified A.C. voltage inputted to and the D.C. voltage outputted by preconditioner control 50. The output of multiplier 100 is supplied to a multiplier, latch, PWM (pulse width modulator), timer and logic circuit 120. Circuit 120 also receives signals from a current sense input (pin 4), a zero current detector (pin 5) through a zero current detector 130 and a D.C. source V_{cc} inputted at pin 8 of chip IC1. The D.C. source V_{cc} prior to being coupled to circuit 120 is processed by an undervoltage lockout 140 and a 2.5 voltage reference 150. The output of circuit 120 is applied as a drive output to pin 7 through an amplifier 160.

As shown in FIG. 2, pin 4 of chip IC1 (i.e. the current sense input) receives a signal having two components, that is, a signal representing current flow through transistor Q1 (i.e. current flowing through resistor R23) and an active offset (i.e. current flowing through diode D_{14} and resistor R30). The active offset is determined by the voltage at a cathode K of chip IC3. Cathode K voltage in turn is determined by the compensating voltage outputted at pin 2 of chip IC1. The compensating voltage reflects the voltage across capacitor CE of FIG. 1 or across capacitors C5', C6' of FIG. 2 (i.e. voltage output of preconditioner 80). As the voltage across capacitor CE of FIG. 1 or capacitors C5', C6' of FIG. 2 rises beyond a predetermined level (e.g. overcharges), cathode K voltage changes from a low level of about 2 volts to a high level of about 11 volts. Cathode K voltage is therefore directly proportional to the output voltage of preconditioner 80 (i.e. cathode voltage rises and lowers as the voltage output of preconditioner 80 rises and lowers, respectively).

In other words, only when the voltage across capacitor CE of FIG. 1 or capacitors C5', C6' of FIG. 2 rises beyond a predetermined level does cathode K voltage of chip IC3 assume a sufficient magnitude resulting in a sufficient offset (current flow) inputted at pin 4 of chip IC1 to significantly quicken the speed at which transistor Q1 turns OFF. The more quickly transistor Q1 turns OFF, the smaller the build up of energy stored within choke L3. Transfer of a limited amount of stored energy by choke L3 to capacitor CE of FIG. 1 or capacitors C5', C6' of FIG. 2 precluding overcharge of such capacitors results.

As compared to conventional power factor controllers which provide a passive (i.e. constant) offset inputted to pin 4 of chip IC1, the active offset in accordance with the invention is of a substantial magnitude only when the voltage across capacitor CE of FIG. 1 or capacitors C5', C6' of FIG. 2 are above a predetermined level (e.g. overcharged). The active offset is of a substantial magnitude only during no-load (including extremely light load) conditions inasmuch as overcharge conditions of capacitor CE of FIG. 1 and capacitors C5', C6' of FIG. 2 do not occur during normal steady state operation of ballast 20.

As shown in FIGS. 2 and 4, cathode K voltage of chip IC3 is determined based on the input voltage applied to a reference R of chip IC3. More particularly, chip IC3 includes a comparator 200 having a non-inverting input to which reference R is connected and an inverting input fed by a 2.5 voltage reference. An anode A of chip IC3 is grounded. The output of comparator 200 is connected to the base of an NPN transistor 210. The collector of transistor 200 is connected to cathode K of chip IC3.

When the voltage applied to reference R is equal to or less than 2.5 volts, transistor 210 is turned OFF. Conversely, when the voltage applied to input R is greater than 2.5 volts, transistor 210 is turned ON. When the voltage across capacitors C5' and C6' is too high (e.g. overcharged during no-load conditions), the compensating voltage outputted at pin 2 of chip IC1 will be less than 2.5 volts. Transistor 210 will be turned OFF. The voltage at cathode K of chip IC3 will be approximately 11 volts resulting in a current flow (offset) of between 40 - 60 microamperes flowing through resistor R30 into pin 4 of chip IC1. The current flowing through resistor R30 significantly offsets the sensed current flowing into pin 4 of chip IC1 through resistor R23 (i.e. representing the current flow through transistor Q1) eventuating in quick turn OFF of transistor Q1.

During normal operation of ballast 20 following ignition of lamp load LL (i.e. steady state operation), the compensating voltage at pin 2 of chip IC1 turns ON transistor 210 of chip IC3. The voltage at cathode K of chip IC3 drops to approximately 2 volts resulting in an offset of approximately 10 microamperes flowing through resistor R30. The speed at which transistor Q1 is turned OFF is not significantly affected based on such a low offset.

By providing a substantial offset only during no-load conditions, chip IC1 enhances (increases) sensitivity to no-load output conditions of preconditioner 80. The invention by recognizing that overcharge conditions across capacitor CE of FIG. 1 and capacitors C5' and C6' of FIG. 2 occur primarily (and normally only) during no-load conditions of ballast 20 provides only a substantial offset during no-load conditions. Consequently, overcharging of capacitor CE of FIG. 1 and capacitors C5' and C6' of FIG. 2 are substantially avoided. By not providing a constant, passive offset, the THD of ballast 20 is substantially reduced as compared to conventional ballasts which incorporate a passive offset in combination with a power factor controller. In particular, by providing an active rather than a passive offset to chip IC1 (i.e. power factor controller), transistor Q1 switches OFF much more quickly only during no-load conditions resulting in an overall lower THD while preventing capacitor CE of FIG. 1 and capacitors C5' and C6' of FIG. 2 from overcharging. Through the enhanced sensitivity to no-load conditions, ballast 20 is able to maintain a relatively constant power factor ranging from about 0.96 to about 0.99. Preferably, although not necessarily, the active offset limits the voltage across preconditioner 80 output to about 525-550 volts whereas without any offset this voltage can rise to about 660 volts.

It will thus be seen that the objects set forth above and those made apparent from the preced-

ing description are efficiently attained and, since certain changes can be made in the above method and construction set forth without departing from the spirit and scope of the invention, it is intended that all matter contained in the above description and shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

It is also to be understood that the following claims are intended to cover all the generic and specific features of the invention herein described and all statements of the scope of the invention, which as a matter of language, might be said to fall therebetween.

Claims

1. A switch mode power supply, comprising:
   a current source for producing current;
   output means responsive to said current for providing an output voltage;
   switch means for conditioning current supplied to said output means;
   control means responsive to a control signal for controlling conditioning by said switch means of current supplied to said output means; and
   sensing means for producing said control signal, said control signal including a sensed signal representing current flow through said switch means and a varying offset based on the output voltage of said output means.

2. The switch mode power supply of claim 1, wherein said current source includes inductor means responsive to said switch means for supplying current to said output means.

3. The switch mode power supply of claim 1, wherein said output means includes at least one capacitor across which said output voltage is applied.

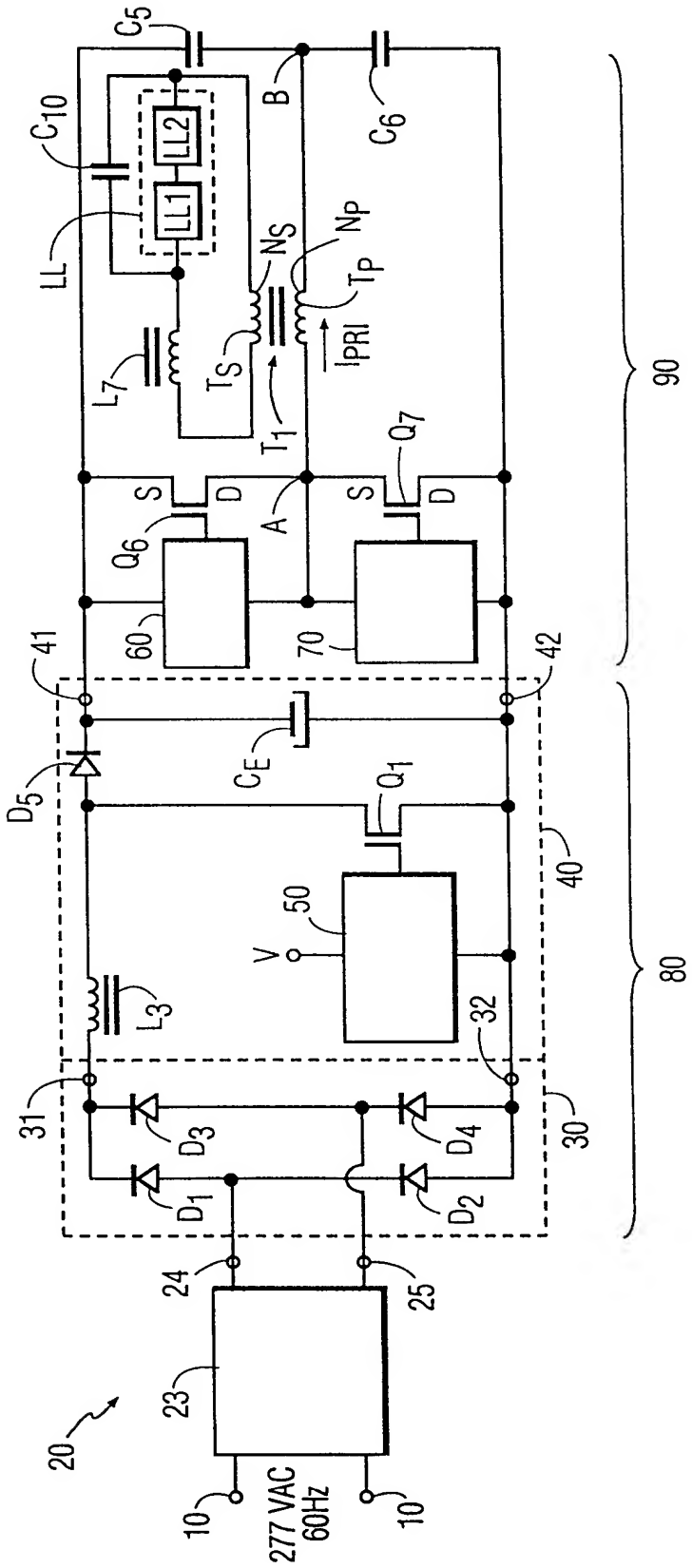
4. A switch mode power supply according to one or more of the previous claims, wherein said control means is a power factor controller serving to control the power supply power factor.

5. A switch mode power supply according to one or more of the previous claims, wherein said offset is directly proportional to said output voltage.

6. A switch mode power supply according to any of the previous claims, wherein said sensing means includes zener diode means having a cathode which varies between a low voltage level and a high voltage level based on the output voltage at said output means.

7. A switch mode power supply according to one or more of the previous claims, wherein the magnitude of said offset varies between two levels.

8. Ballast for operating a discharge lamp comprising a switch mode power supply according to one or more of the previous claims.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L3
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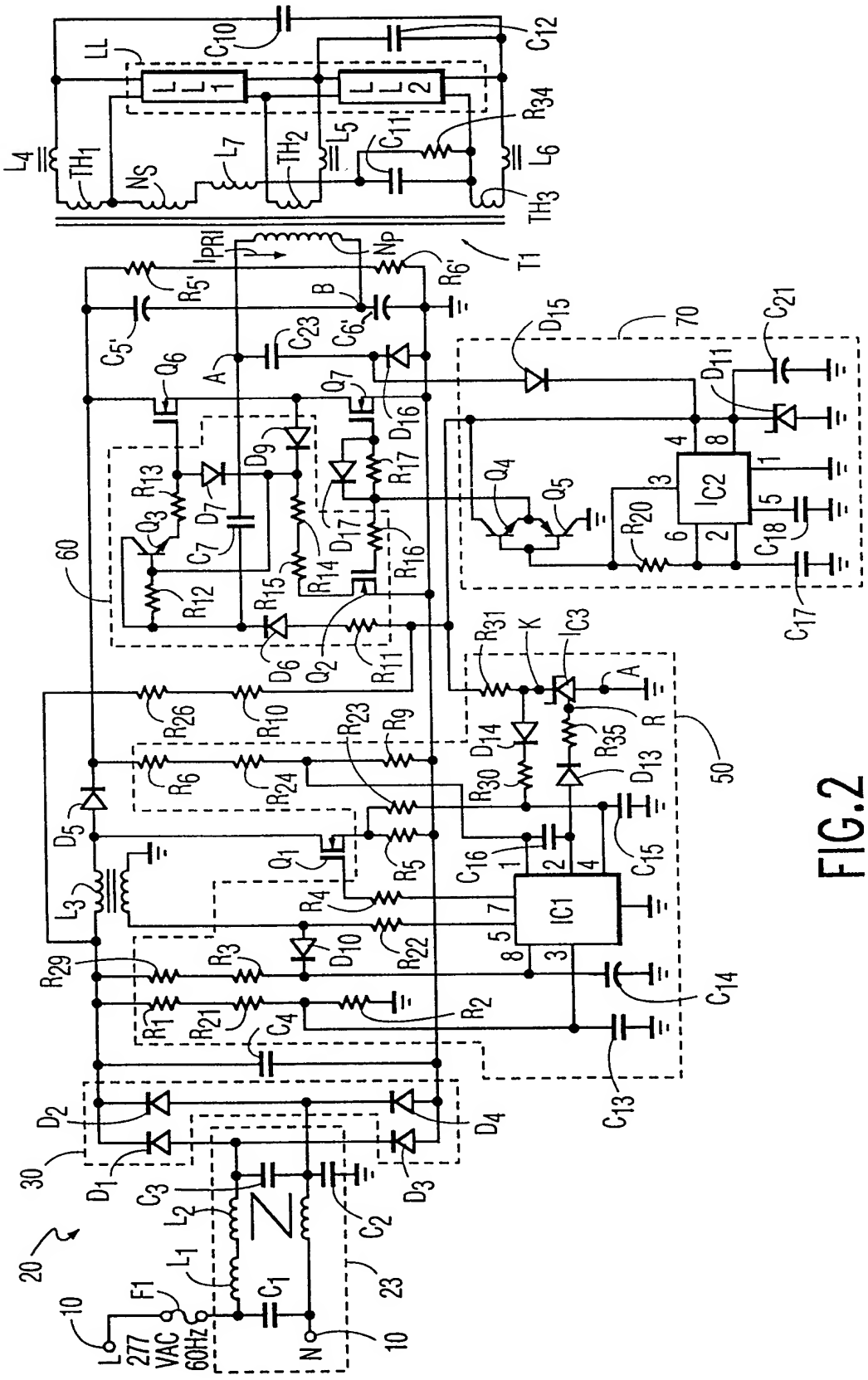
FIG. 1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D4
30
D1
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FIG.2

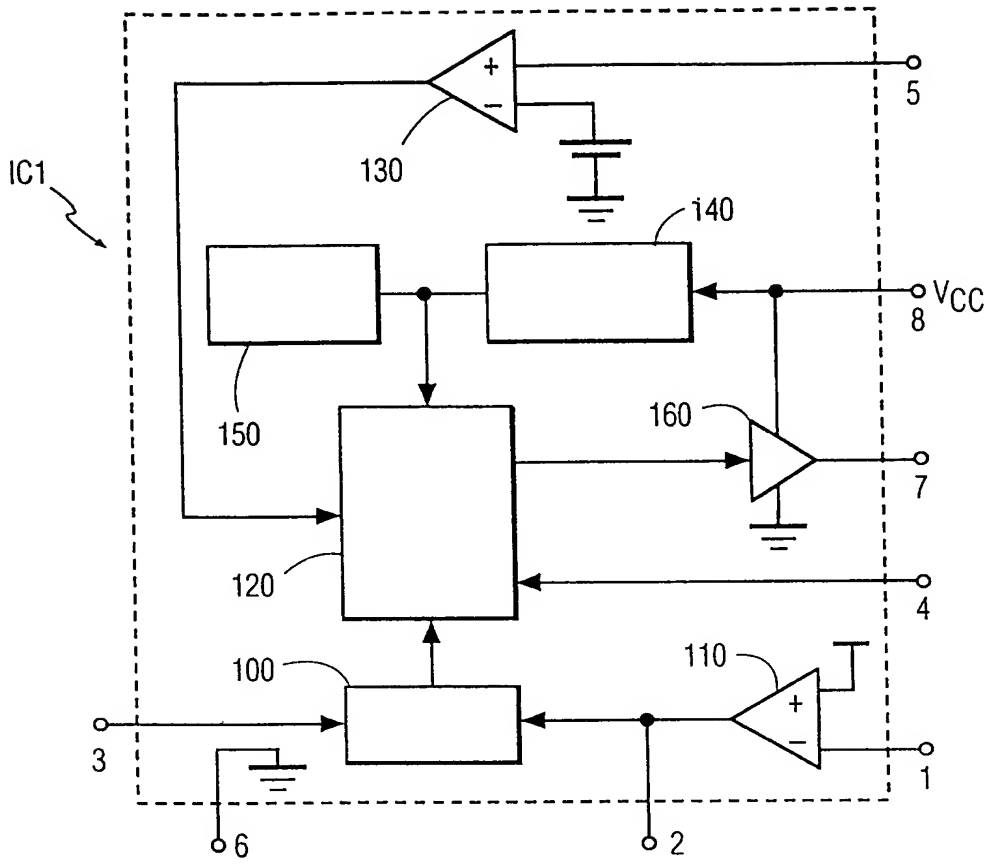

FIG.3

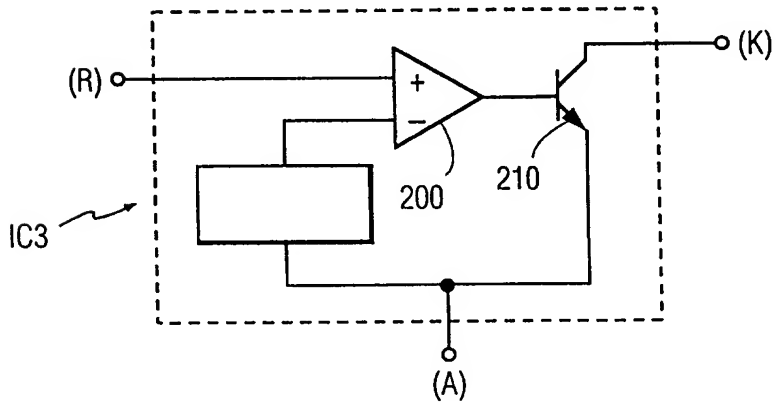

FIG.4